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Title: GATE ARRAY ARCHITECTURE
1st Named Inventor: Brian D. Possley
Application No.: 09/902,912
Docket No.: 42390P6643C
Sheet: 1 of 7

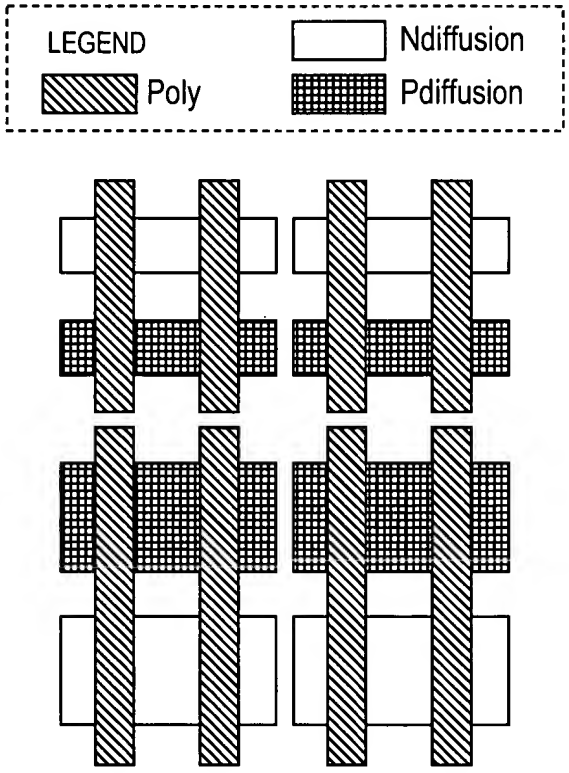
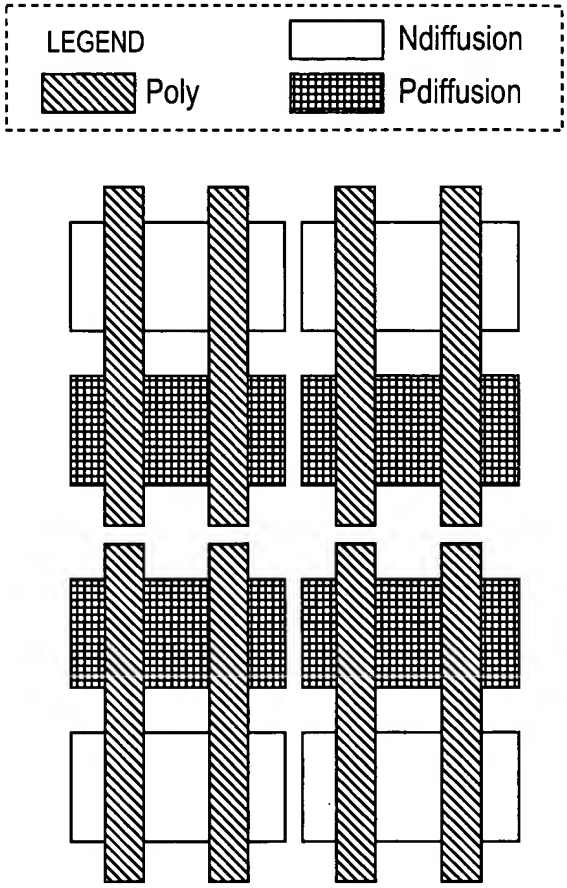


FIG. 1



Traditional Approach

FIG. 2

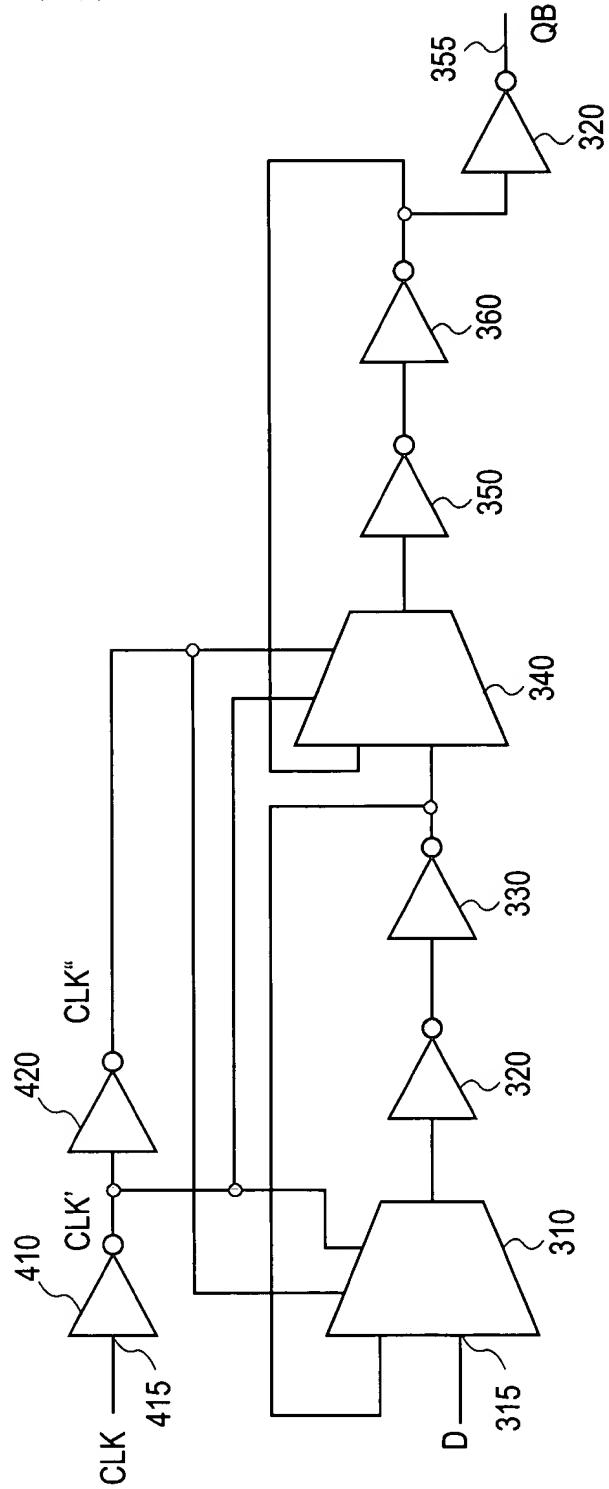


FIG. 3

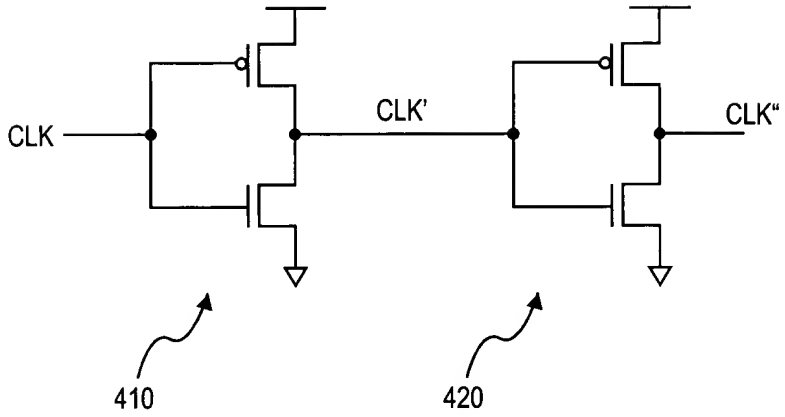


FIG. 4

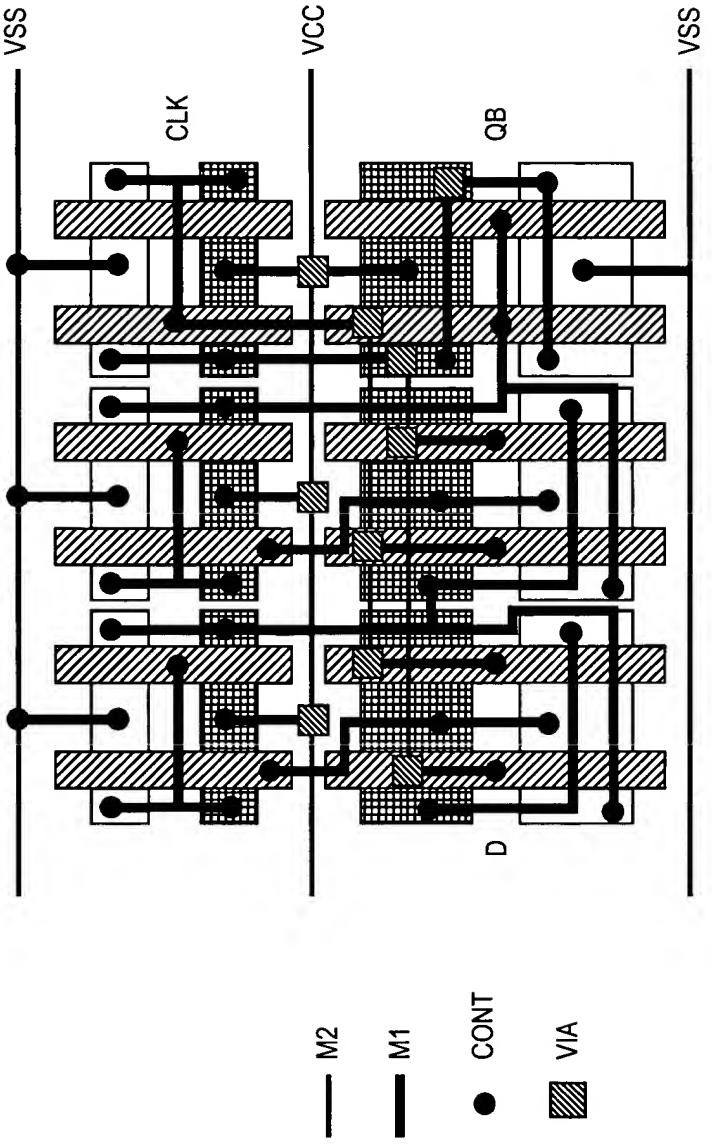


FIG. 5

Table 1

Name	Clock Pin Power	Notes
Capacitance Improved	0.06 pJ	FIG. 2
Si Arc	0.13 pJ	SiArc CBA
Traditional	0.15 pJ	FIG. 2

pJ = pico joules

FIG. 6

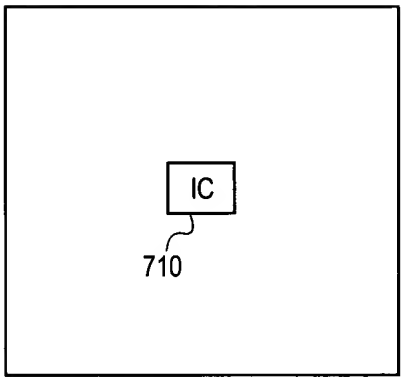


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FIG. 7